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Docket No. BUR9-2003-0026-US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICEApplicant: Gardecki *et al.*

Group Art Unit: 2823

Filed: 6/28/2003

Examiner: Kebede, Brook

Serial No.: 10/604,164

Title: **METHOD FOR FORMING INTERCONNECTS ON THIN WAFERS**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

RESTRICTION ELECTION

In response to the Restriction Requirement dated August 20, 2004, Applicants hereby provisionally elect Group I, claims 1-24, drawn to method for forming a semiconductor interconnect, classified in class 438, subclass 113. This election is made with traverse, and Applicants hereby reserve the right to file a divisional application in connection with unelected claims 25-28, drawn to wafer holder apparatus.

With regard to the Restriction Requirement, Applicants respectfully submit that the subject matter of all claims 1-28 is sufficiently related that a thorough search for the subject matter of any one group of claims would encompass a search for the subject matter of the remaining claims. Thus, Applicants respectfully submit that the search and the examination of the entire application could be made without serious burden. See MPEP § 803, in which it is stated that "if the search and examination of the entire application can be made without serious burden,

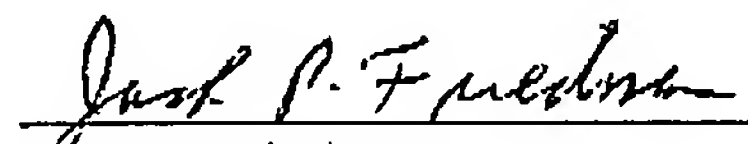
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the Examiner must examine it on the merits, even though it includes claims to independent or distinct inventions" (emphasis added). Applicants respectfully submit that this policy should apply in the present application in order to avoid unnecessary delay and expense to Applicants and duplicative examination by the Patent Office.

Should the Examiner require or request anything further from Applicants prior to examination, the Examiner is requested to contact Applicants' undersigned representative at the telephone number below. Otherwise, Applicants request early and favorable examination on the merits.

Date: 08/26/2004


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